HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Docket No.: 10002929-3
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Jeffrey C. Swanson et al.

Application No.: 10/670,620 | Confirmation No.: 6729

Filed: September 25, 2003 | Art Unit: 2113

For: A SYSTEM AND METHOD FOR MULTIPLE CYCLE CAPTURE OF CHIP STATE | Examiner: M. C. Maskulinski

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on October 12, 2006, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

Hewlett-Packard Development Company, L.P., a Limited Partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249, Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 20 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 21

2. Claims withdrawn from consideration but not canceled: None

3. Claims pending: 1-20

4. Claims allowed: 17, 18 and 20

5. Claims rejected: 1-16 and 19

C. Claims On Appeal

The claims on appeal are claims 1-16 and 19.

IV. STATUS OF AMENDMENTS

Appellant did not file an Amendment After Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

According to independent claim 1, circuitry for providing external access to signals that are internal to an integrated circuit comprises a network (*e.g.*, 100 of FIGURE 1) comprising a plurality of multiplexers (*e.g.*, 102, 104, 106, 108, 100 of FIGURE 1) physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit (*e.g.*, page 12, line 5 through page 13, line 9); a trigger event generator (*e.g.*, 300 of FIGURE 3) receiving a first N bits of sampled data from said network, said trigger event generator including a definable mask and selectively performing a boolean operation on said sampled data based on said mask to provide a trigger event (*e.g.*, page 15, line 9 through page 16, line 2); and a FIFO storage array (*e.g.*, 500 of FIGURES 3 and 8) that stores at least a portion of the sampled data (*e.g.*, page 3, lines 7-24).

According to claim 3, the circuitry according to claim 1 further comprises a counter providing an intermediate trigger in response to a predetermined number of the trigger events (*e.g.*, 1018 and 1024 of FIGURE 10 and, page 8, lines 1-19, page 9, lines 1-7, and page 17, lines 25-27).

According to claim 13, target data comprises said first N bits of sampled data supplied by said network (*e.g.*, page 23, lines 13-24).

According to claim 14, said target data consists of a second N bits of sampled data supplied by said network (*e.g.*, page 23, lines 13-24).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-3, 12-16 and 19 are rejected under 35 U.S.C. §102(b) over US 5,867,644 (hereinafter, *Ranson*).

2. Claims 4-11 are rejected under 35 U.S.C. §103(a) over *Ranson* in view of US 5,711,240 (hereinafter, *Tobin*).

The double patenting rejection is not addressed herein, as Appellant has agreed to file a terminal disclaimer upon allowance of the claims.

VII. ARGUMENT

A. First Ground of Rejection

On pages 6-9 of the Final Action , claims 1-3, 12-16 and 19 are rejected under 35 U.S.C. §102(b) over *Ranson*. Appellant traverses the rejection.

To anticipate a claim under 35 U.S.C. § 102, a reference must teach every element of the claim. *See Verdegaal Bros. Inc. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Moreover, in order for an applied reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim." *See Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989). Furthermore, in order for a reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he elements must be arranged as required by the claim." M.P.E.P. § 2131, citing *In re Bond*, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). As discussed further below, these requirements are not satisfied by the 35 U.S.C. § 102 rejection because *Ranson* does not teach every element of the claims.

1. Claims 1, 2, 12, 15, 16, and 19

Claim 1 recites, in part, "a FIFO storage array that stores at least a portion of the sampled data." The Final Action cites *Ranson* at FIGURE 4 and the passage at column 13, line 38 through column 14, line 62 to teach the feature. Final Action at 7. The passage at columns 13-14 describes, among other things, the contents of FIGURES 6, 7, 9, and 10. However, the passage does not teach, or even mention, a FIFO storage array. These portions of *Ranson* do not teach the feature because they do not teach a FIFO (First-In-First-Out) storage array. For instance, FIGURE 4 shows a "staging register" and "remote registers," but does not teach that any of those registers are FIFOs. A register, by itself, is not enough to teach a FIFO, and FIGURE 4 is not sufficient to teach the feature in as complete detail as is contained in the claim.

In the Response to Arguments section of the Final Action, the Examiner asserts that the registers of FIGURE 4 are a FIFO storage array based upon the way that *Ranson* describes shifting the data. Final Action at 12. Specifically, the Examiner points to the passage beginning at column 13, line 39, and ending at column 14, line 12, and alleges that the registers must be FIFO registers because the passage describes shifting data header-first. *Id.* In other words, the Examiner assumes that since "headers are always at the beginning of data" and since data is shifted header-first in the system of FIGURE 4, that the registers must receive the data header-first and also shift the data out in the same order that it was received. However, the Examiner assumes too much.

A review of the process described in the cited passage of *Ranson* clarifies the issue. It appears that the Examiner equates the contents of staging register 500 with "data" and the contents of header generation register 504 with a data header. *See Ranson* at Col. 13, lines 39-56. *Ranson* teaches that microprocessor 100 loads the contents of header generation register 504 and moves the contents of one general purpose register into staging register 500. *Id.* at lines 25-35. Specifically, staging register 500 is loaded in step 706, and header generation register 504 is loaded in step 708. *Id.* at lines 39-50. Then, the contents of header generation register 504 are shifted on to serial data line 410 before the contents of staging register 500 are shifted onto line 410. *Id.* at Col. 13, line 57, through col. 14, line 1.

The Examiner's assertion that the process described above teaches shifting in a FIFO manner is incorrect for at least two reasons. First, as described above, FIFO means "First-In-First-Out," which does not necessarily flow from the cited passage. Specifically, it appears that staging register 500 is loaded before header generation register 504 is loaded, while the contents of header generation register 504 are shifted out before the contents of staging register 500 are shifted out. This does not teach shifting "in a FIFO manner," as asserted by the Examiner.

Second, it appears the Examiner is assuming that the data and header are loaded into and shifted out of the same register, and that the header is loaded into the one register first and is followed by the loading of the data. However, as shown above, the data and header are loaded into different registers in a different order from that described by the Examiner. Thus, the Examiner's assumption does not hold. Accordingly, the cited portions of *Ranson* do not teach the above-recited feature of claim 1. Since the cited portions of *Ranson* do not teach a FIFO storage array, the rejection must fail.

Dependent claims 2, 12, 15, 16, and 19 each depend either directly or indirectly from independent claim 1 and, thus, inherit all of the limitations of independent claim 1. Thus, *Ranson* does not teach all claim limitations of claims 2, 12, 15, 16, and 19. It is respectfully submitted that dependent claims 2, 12, 15, 16, and 19 are allowable at least because of their dependence from claim 1 for the reasons discussed above. Accordingly, Appellant respectfully requests the reversal of the 35 U.S.C. § 102 rejection of claims 1, 2, 12, 15, 16, and 19.

2. Claim 3

In addition to being allowable because of its dependence from claim 1, claim 3 recites, in part, "a counter providing an intermediate trigger in response to a predetermined number of said trigger events." The cited portion of *Ranson* does not appear to teach this feature of claim 3 because it does not appear to teach taking an action in response to a predetermined number of trigger events. The Final Action cites *Ranson* at column 3, lines 55-58 to teach the feature. Final Action at 8. The cited passage teaches that output from counters (that indicate the occurrence of user-definable events) can be used as state machine input or can be used to generate triggers. *Ranson* at Col. 3, lines 52-60. However, the cited

passage does not teach taking an action in response to a predetermined number of trigger events, much less providing an intermediate trigger in response to a predetermined number of trigger events. In fact, the cited portion does not mention counting trigger events at all. Accordingly, the cited portion of *Ranson* does not teach the above-recited feature of claim 1. Thus, Appellant respectfully requests the reversal of the 35 U.S.C. § 102 rejection of claim 3.

3. Claims 13 and 14

In addition to being allowable because of its dependence from claim 1, claim 13 recites, in part, "said target data comprises said first N bits of sampled data supplied by said network." Additionally, claim 14 recites, in part, "said target data consists of a second N bits of sampled data supplied by said network." The cited portion of *Ranson* does not teach these features of claims 13 and 14 at least because it does not appear to teach that target data comprises or consists of bits of sampled data. Note that claim 1, from which claims 13 and 14 depend, recites that the trigger event generator receives sampled data from the network and selectively performs a boolean operation on the sampled data to provide a trigger event. Further, claim 12, from which claims 13 and 14 depend, recites that a sampling circuit is responsive to the trigger event to identify the target data. However, the cited portion of *Ranson* does not appear to teach a relationship between sampled data and target data wherein the target data comprises or consists of sampled data, as recited in claims 13 and 14. Accordingly, the cited portion of *Ranson* do not teach the above-recited feature of claims 13 and 14. Thus, Appellant respectfully requests the reversal of the 35 U.S.C. § 102 rejection of claims 13 and 14.

B. Second Ground of Rejection

On pages 9-11 of the Final Action, claims 4-11 are rejected under 35 U.S.C. §103(a) over *Ranson* in view of *Tobin*. Appellant traverses the rejection.

To show obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the applied reference. *See In re Vaeck* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. *In re Merck and Co., Inc.,* 800 F.2d 1091, 231

USPQ 375 (Fed. Cir. 1986). Finally, the applied reference must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Without conceding any other criteria, Appellant respectfully asserts that the rejection does not satisfy the third criterion, as discussed further below.

As shown above, the cited portions of *Ranson* do not teach every feature of independent claim 1. Dependent claims 4-11 each depend either directly or indirectly from independent claim 1 and, thus, inherit all of the limitations of independent claim 1. Thus, *Ranson* does not teach or suggest all claim limitations of claims 4-11. Further, *Tobin* does not teach or suggest the missing features, nor is *Tobin* used by the Final Action to supply the missing features. It is respectfully submitted that dependent claims 4-11 are allowable at least because of their dependence from claim 1 for the reasons discussed above. Accordingly, Appellant respectfully requests the reversal of the 35 U.S.C. § 103 rejection of claims 4-11.

VIII. CLAIMS APPENDIX

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE APPENDIX

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included.

Appellant believes a fee of $500 is due with this response. However, if additional fees are due, please charge our Deposit Account No. 08-2025, under Order No. 10002929-3 from which the undersigned is authorized to draw.

Respectfully submitted,

By: _____

Michael A. Papalas
Attorney/Agent for Applicant(s)
Reg. No. 40,381
Date: December 12, 2006
Telephone No. (214) 855-8186

APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/670,620

1. Circuitry for providing external access to signals that are internal to an integrated circuit, said circuitry comprising:

a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit;

a trigger event generator receiving a first N bits of sampled data from said network, said trigger event generator including a definable mask and selectively performing a boolean operation on said sampled data based on said mask to provide a trigger event; and

a FIFO storage array that stores at least a portion of the sampled data.

2. The circuitry according to claim 1 wherein said trigger event generator further comprises a switch for selectively providing, as said trigger event, one of (i) a result of said boolean operation on said sampled data, (ii) a performance counter event signal, and (iii) an externally applied trigger signal.

3. The circuitry according to claim 1 further comprising a counter providing an intermediate trigger in response to a predetermined number of said trigger events.

4. The circuitry according to claim 3 further comprising a trigger delay providing a sample command a predetermined number of cycles following said intermediate trigger.

5. The circuitry according to claim 4 wherein said predetermined number of cycles represent respective operating cycles of the integrated circuit.

6. The circuitry according to claim 4 wherein said predetermined number of cycles represent respective machine clock cycles.

7. The circuitry according to claim 4 further comprising a programmable register storing a value corresponding to said predetermined number of cycles.

8. The circuitry according to claim 7 wherein said programmable register selectively increments said value corresponding to said predetermined number of cycles by a predetermined number of said cycles.

9. The circuitry according to claim 4 further comprising a sampling circuit responsive to said sample command to identify target data.

10. The circuitry according to claim 1 further comprising a trigger delay providing a sample command a predetermined number of cycles following said trigger event.

11. The circuitry according to claim 10 further comprising a sampling circuit responsive to said sample command to identify target data.

12. The circuitry according to claim 1 further comprising a sampling circuit responsive to said trigger event to identify target data.

13. The circuitry according to claim 12 wherein said target data comprises said first N bits of sampled data supplied by said network.

14. The circuitry according to claim 12 wherein said target data consists of a second N bits of sampled data supplied by said network.

15. The circuitry according to claim 12 wherein said sampling circuit includes a memory storing said target data.

16. The circuitry according to claim 12 wherein said sampling circuit includes switching circuitry configured to selectively provide a predetermined portion of said target data.

17. Circuitry for providing external access to signals that are internal to an integrated circuit, said circuitry comprising:

a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit;

a trigger event generator receiving a first N bits of sampled data from said network, said trigger event generator including a definable mask and selectively performing a boolean operation on said sampled data based on said mask to provide a trigger event; and

a sampling circuit responsive to said trigger event to identify target data, wherein said sampling circuit includes switching circuitry configured to selectively provide a predetermined portion of said target data, wherein said predetermined portion of said target data is N/M bits wide where N/M is a positive integer.

18. The circuitry according to claim 17 wherein said sampling circuit includes multiplexing circuitry configured to combine M of said portions of said target data into a data unit N bits wide.

19. The circuitry according to claim 12 wherein said sampling circuit includes a FIFO storage array.

20. Circuitry for providing external access to signals that are internal to an integrated circuit, said circuitry comprising:

a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit;

a trigger event generator receiving a first N bits of sampled data from said network, said trigger event generator including a definable mask and selectively performing a boolean operation on said sampled data based on said mask to provide a trigger event; and

a sampling circuit responsive to said trigger event to identify target data, wherein said sampling circuit includes a FIFO storage array, and wherein said FIFO storage array is N/M bits wide where N/M is a positive integer.

APPENDIX B

Evidence. None

APPENDIX C

Related Proceedings. None